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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
DAVID W. SMITH

Serial No.: 09/225,388

Filed: JANUARY 5, 1999

For: METHOD AND APPARATUS FOR PATTERN MATCHING ON SINGLE AND MULTIPLE PATTERN STRUCTURES

Group Art Unit: 2665

Examiner: TOAN D. NGUYEN

Atty. Dkt.: 2000.002500/TT2581

CUSTOMER NO. 23720

APPEAL BRIEF

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8	
DATE OF DEPOSIT:	August 30, 2006

I hereby certify that this paper or fee is being deposited with the United States Postal Service with sufficient postage as "FIRST CLASS MAIL" addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Nancy Nolan
Signature

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

On June 29, 2006, Appellant filed a Notice of Appeal in response to a Final Office Action dated April 3, 2006, issued in connection with the above-identified application. In support of the appeal, Appellant hereby submits this Appeal Brief to the Board of Patent Appeals and Interferences.

Since the Notice of Appeal for the present invention was received and stamped by the USPTO Mailroom on July 3, 2006, the two-month date for filing this Appeal Brief is Monday, September 4, 2006 (since September 3, 2006 falls on a Sunday). This Appeal Brief is being filed on August 30, 2006, therefore, it is timely filed.

If an extension of time is required to enable this paper to be timely filed and there is no separate Petition for Extension of Time filed herewith, this paper is to be construed as also constituting a Petition for Extension of Time Under 37 CFR § 1.136(a) for a period of time sufficient to enable this document to be timely filed.

The Commissioner is authorized to deduct the fee for filing this Appeal Brief ($500.00) from Williams Morgan & Amerson, P.C. Deposit Account No. 50-0786/2000.002500. No other fee is believed to be due in connection with the filing of this document. However, should any fee under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to this document, the Commissioner is hereby authorized to deduct said fee from Williams Morgan & Amerson, P.C. Deposit Account No. 50-0786/2000.002500.

I. REAL PARTY IN INTEREST

The present application is owned by Advanced Micro Devices, Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellant is not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

III. STATUS OF CLAIMS

Claims 1-35 remain pending in this application.

Claims 1-2, 9, 23-24, 31-32 and 34 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,802,305 (***McKaughan***), in view of U.S. Patent No. 6,098,100 ***(Wey)***.

Claims 3-6, 8, 10-18, 20-22, 25-28, 30, 33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***McKaughan*** in view of ***Wey*** and further in view of ***Warren***.

IV. STATUS OF AMENDMENTS

After the Final Rejections, no other amendments were made to any other claims.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention facilitates a true low-power mode for host systems, such as computers, while maintaining capabilities of receiving and processing data from outside sources, such as network lines. These capabilities can be achieved by employing hardware circuitry, rather than relying upon pure software solutions, to monitor incoming data. By utilizing the hardware solution presented in the present invention, the host circuitry (150) can achieve an actual low-power mode, since it will not be responsible for monitoring incoming data. Furthermore, since software residing in the host will not be used to detect and decode incoming data, the host only has to enter a wake-up mode upon a signal from the hardware. See Specification, page 8, lines 16-22.

The present invention provides a method for detecting and decoding data to wake up a host circuitry (150). A set of data signals is received from an external data source (110). A size of said received set of data signals is detected to use as a factor for decoding said data. The received set of data signals is decoded. A destination address from said set of data signals is extracted. The destination address extracted from said data signals is compared to a known data value. A determination is made as to whether said received data signals should be received by a host circuitry (150) based upon said comparison of said destination address extracted from said data signals to said known data value. At least one status signal alerting said host circuitry (150)

of said determination that said received data signals should be received by said host circuitry (150) is generated. The host circuitry (150) is awakened from a sleep mode upon a determination that said received set of data is addressed to said host circuitry (150). *See* Figure 1; Specification, page 9, lines 1-19; page 10, lines 15-23.

The present invention also provides an apparatus for detecting and decoding data to wake up a host circuitry (150). The apparatus includes means for receiving a data signal and means for detecting a size of said received data signal. The apparatus also includes a data formatter (220), a clock divider (230), a counter (240), and a host circuitry interface (245) capable of transmitting and receiving data from a host circuitry (150). The host circuitry (150) enters a wake up state from a sleep mode based upon decoded address data received by said host circuitry (150). The decoded address data is based upon a content of said data signal and said size of said received data signals. The apparatus also includes a memory circuitry (250), a plurality of comparators (260), a mask circuitry (270), a digital logic circuitry (265), a plurality of status registers (280), and a plurality of clocked registers (285). *See* Figures 2 and 3; Specification, page 10, line 24-page 12, line 16.

The present invention also provides a computer readable program storage device encoded with instructions that, when executed by a computer, performs a method for detecting and decoding data to wake up a host circuitry (150). The method includes: receiving a set of data signals from an external data source (110); detecting a size of said received set of data signals to use as a factor for decoding said data signals; decoding said received set of data signals; extracting a destination address from said set of data signals; comparing said destination address extracted from said data signals to a known data value; determining whether said received data signals should be received by a host circuitry (150) based upon said comparison of said

destination address extracted from said data signals to said known data value; generating at least one status signal alerting said host circuitry (150) of said determination that said received data signals should be received by said host circuitry (150); and waking up said host circuitry (150) from a sleep mode upon a determination that said received set of data is addressed to said host circuitry (150). *See* Figure 1; Specification, page 9, lines 1-19; page 10, lines 15-23.

The present invention provides a method for detecting and decoding data to wake up a host circuitry (150). A data signal is received. A size of said received data signal is detected to use as a factor for extracting a destination address. The destination address is extracted based upon said data signal to determine whether a host circuitry (150) is being addressed by comparing said destination address to a predetermined address. The host circuitry (150) is woken from a sleep mode based upon said determination that said host circuitry (150) is being addressed. *See* Figure 1; Specification, page 9, lines 1-19; page 10, lines 15-23.

The present invention provides an apparatus for detecting and decoding data to wake up a host circuitry (150). The apparatus includes a controller (130) that is adapted to: receive a data signal; detect a size of said received set of data signals to use as a factor to extract a destination address; extract said destination address based upon said data signal to determine whether a host circuitry (150) is being addressed by comparing said destination address to a predetermined address; and wake up said host circuitry (150) from a sleep mode based upon said determination that said host circuitry (150) is being addressed. *See* Figures 1 and 3; Specification, page 9, lines 1-19; page 12, line 18-page 15, line 18; page 17, line 9-page 19-, line 12.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether claims 1-2, 9, 23-24, 31-32 and 34 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,802,305 (***McKaughan***), in view of U.S. Patent No. 6,098,100 ***(Wey)***; and

2. Whether claims 3-6, 8, 10-18, 20-22, 25-28, 30, 33 and 35 stand rejected under 35 U.S.C. § 103(a) as being patentable over ***McKaughan***, in view of ***Wey*** further in view of U.S. Patent 4,516,201 ***(Warren)***.

VII. ARGUMENT

The present invention is directed to detecting and decoding data for waking up a host circuitry from a sleep mode. The present invention provides for receiving data signals from an external source and detecting the size of the received set of data signal for use as a factor for decoding the data. Upon decoding the data, destination address is extracted from the data signals and the destination address is compared to a known data value. The present invention provides for determining whether the received data signals should be received by a host circuitry based upon this comparison. A status signal alerting the host circuitry of the determination that the data signal should be received by the host circuitry is generated. The present invention provides for waking up the host circuitry from a sleep mode based upon a determination that the received set of data is addressed to the host circuitry. The Examiner relies heavily on U.S. Patent No. 5,802,305 (***McKaughan***) and U. S. Patent No. 6,098,100 (***Wey***). However, the Examiner has failed to provide a *prima facia* showing of obviousness of the claims of the present invention based upon the cited prior art. ***McKaughan*** refers to a computer network that contains a

plurality of interconnected computers, wherein a network interface card associated with the sleeping computers detects incoming packets and compares the incoming packets to a list of packets stored in the interface cards. However, ***McKaughan*** does not disclose detecting the size of the received set of data signals to use as a factor for decoding the data, as called for by claims of the present invention. ***Wey*** does not make up for this deficit. ***Wey*** simply discloses determining whether the value of a pattern counter has reached a required pattern length based on incoming signals. ***Wey*** discloses that the determination made when the pattern counter has reached a pattern length is merely referring to whether a particular number of pattern matches have been detected and whether all of the pattern register data has been matched. This inquiry may be independent of the size of the data that comes in since several bites of incoming data may or may not match. In other words, ***Wey*** is interested only in the number of pattern matches. Therefore, neither ***McKaughan*** nor ***Wey*** discloses detecting the size of the data for use as a factor of decoding data. Additionally, there are various other elements of claims of the present invention that are not disclosed by the cited prior art.

The specific claims of the present invention are discussed below.

A. Claims 1-2, 9, 23-24, 31-32 and 34 Are Not Rendered Unpatentable under 35 U.S.C. § 103(a) by *McKaughan* (U.S. Patent No. 5,802,305) in view of *Wey* (U.S. Patent No. 6,098,100)

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine reference teachings. Third, there must be a reasonable expectation of success. The

teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Appellant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. Moreover, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988); M.P.E.P. § 2143.03.

With respect to the alleged obviousness, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Health-care Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. The consistent criterion for determining obviousness is whether the prior art would have suggested to one of ordinary skill in the art that the process should be carried out and would have a reasonable likelihood of success viewed in the light of the prior art. Both the suggestion and the expectation of success must be founded in the prior art, not in the Appellant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991; *In re O'Farrell*, 853 F.2d 894 (Fed. Cir. 1988); M.P.E.P. § 2142.

Appellant respectfully asserts that the Examiner did not meet the legal standards to reject the claims of the present invention under 35 U.S.C. § 103(a) because the prior art references (***McKaughan*** and ***Wey***) do not teach or suggest all the claim limitations of the claims of the

present invention. Additionally, the Examiner has not provided sufficient evidence or arguments that there is a suggestion that one skilled in the art would have been motivated to combine the references (***McKaughan*** and ***Wey***). In fact, Appellant provides arguments that ***McKaughan*** and ***Wey*** would not have been combined by one skilled in the art. Therefore, the Examiner did not meet the legal standards to establish a *prima facie* case for obviousness under 35 U.S.C. § 103(a) with regarding to claims 1-2, 9, 23-24, 31-32 and 34 under 35 of the present invention.

The Examiner rejected claims 1-2, 9, 23-24, 31-32 and 34 under 35 U.S.C. 103(a) as being unpatentable over ***McKaughan*** (US 5,802,305) in view of ***Wey*** (US 6,098,100). Appellant respectfully traverses the rejections.

Appellant respectfully asserts that ***McKaughan***, in combination with ***Wey***, does not teach, disclose, or suggest all of the elements of claims 1-2, 9, 23-24, 31-32 and 34 under 35 of the present invention. As described in detail below, ***McKaughan***, ***Wey***, nor their combination disclose or make obvious various elements of the claims, including detecting the size of the data for use as a factor for decoding data.

In the Final Office Action dated April 3, 2006, the Examiner argued that ***Wey*** discloses detecting the size of the received data set of signal and cited Figure 2, Reference S15 of ***Wey*** to support this assertion. However, this citation merely refers to comparing the data byte in a frame buffer 10 in ***Wey*** with a data bite in a pattern register 17. ***Wey*** is directed to determining whether a match was detected such that the control logic would then increment the pattern counter 16. This is designed to increment a pattern counter and not detected to determine the size of the data. If sufficient count is detected by the pattern counter 16, the wake up sequence is performed. The Examiner misinterprets this event as detecting the size of the data. The pattern counter 16 of ***Wey*** may be incremented based on matching of the frame buffer data to a particular data in a

pattern register, not necessarily to the size of the data. ***Wey*** merely refers to number of matches between frame buffer data and pattern register data, and not to the size of the data. Therefore, ***Wey*** does not disclose detecting the size of the received data signal in contradiction to the Examiner's assertion. Therefore, the element upon which the Examiner claims is made obvious by the disclosure of ***Wey*** is indeed, not made obvious, and therefore, the combination of ***Wey*** and ***McKaughan*** does not teach, disclose or suggest all of the elements of claims of the present invention, as described in further details below.

McKaughan in combination with ***Wey*** does not teach, disclose or make obvious all of the elements of claim 1 of the present invention. ***McKaughan***, which is the primary reference, does not disclose or make obvious several elements of claim 1 of the present invention, and ***Wey*** does not make up for the deficit of ***McKaughan***. ***McKaughan*** refers to a computer network that contains a plurality of interconnected computers, wherein a network interface card of sleeping computers detects an incoming packet and compares the incoming packet to a list of packets stored on the network interface cards. ***McKaughan*** then compares the received packet to a list of packets on the card and provides a wake-up sequence of a remote computer (see column 6, lines 43-64 of ***McKaughan***). However, ***McKaughan*** does not disclose detecting the size of the received set of data signals as called for by claim 1 of the present invention. ***McKaughan*** merely discloses detecting an incoming packet over a network and filtering the incoming packet with a comparison mask. This does not make obvious the element of detecting the size of the received set of signals or other elements of claim 1. ***McKaughan*** does not disclose detecting the size of the received set of signals. Therefore, Appellant respectfully asserts that among other elements, ***McKaughan*** simply does not disclose or make obvious the element of detecting the size of the received set of signals when determining whether to wake up the computer.

The Examiner cited Figure 4 and related text to support an assertion that ***McKaughan*** discloses or makes obvious the elements called for by claim 1. Appellant respectfully asserts that neither the cited portion of ***McKaughan***, nor any other part of ***McKaughan***, discloses detecting the size of the received set of data signals in the context of determining whether the received data signal should be received by the host circuit and waking up the whole circuitry as called for by claim 1 of the present invention. Figure 4 merely refers to filtering the incoming packet, comparing the resulting filtered incoming packet to the corresponding packet in a list stored on a network interface card and making a decision whether to wake up the computer. *See* Figure 4 and col. 8, lines 45-47, col. 9, lines 3-13 of ***McKaughan***. ***McKaughan*** does not disclose detecting the size of the received set of signals when determining whether to wake up the computer, which is an element called for by claim 1. Further, ***Wey*** does not make up for the deficits of ***McKaughan***.

The Examiner admits that ***McKaughan*** does not disclose detecting a size of the received set of data signals to use as a factor for decoding the data. Appellant respectfully asserts that the Examiner is correct in the statement but, further, ***McKaughan*** does not disclose or make obvious other elements of claim 1 of the present invention. Regarding detecting the size of the data received, ***Wey*** does not make up for this deficit. The Examiner cites ***Wey*** to make obvious this element, however, ***Wey*** does not disclose detecting a size of the received set of data to use as a factor for decoding, as called for by claim 1 of the present invention. The Examiner cites Figure 2, block S18, which refers to the determination whether the pattern counter has reached a pattern length. Upon analysis of the disclosure of ***Wey***, it is abundantly clear that ***Wey*** is not referring to detecting the size of the data. In fact, ***Wey*** discloses that the step S18 relates to determining whether the value of the pattern counter has reached the required pattern length, which relates to the end of the pattern register 17. *See* column 2, line 35-37 of ***Wey***. This is a reference to the

pattern counter which maintains a count each time data in the frame buffer data is matched with the data in the pattern register. *See* step S15 of Figure 2. ***Wey*** discloses that a comparator 14 compares the data byte in the frame buffer 10 with a data byte in the pattern register 17. *See* column 2, lines 22-25. ***Wey*** discloses that, if a match was detected, the control logic increments the value in the pattern counter 16. *See* column 2, lines 31-35. Upon a determination that the sufficient count is detected by the pattern counter 16, the wake up sequence is performed. However, there is no disclosure in ***Wey*** or in ***McKaughan*** to suggest determining the size of the data to use as a factor for decoding the data.

This disclosure of ***Wey*** is abundantly clear that it does not actually examine the size of the data for decoding. ***Wey*** merely determines whether a particular data in the frame buffer matches a byte of data in the pattern register and then increments a counter. When ***Wey*** discloses that the determinations made whether the pattern counter has reached a pattern lend, it is referring to whether a particular number of patterns matches have been detected and whether the all of the pattern register data has been matched. However, this inquiry may be independent as to the size of the data that comes in since several bytes of incoming data may or may not match. Hence, the pattern matching process of ***Wey*** is independent of the size of the incoming data. Accordingly, ***Wey*** simply does not disclose or make obvious the element of detecting the size of the data to use as a factor for decoding the data, as called for by claim 1 of the present invention.

As described above, ***McKaughan*** does not disclose detecting the size of the data at all, much less detecting the size of the data to use as a factor for decoding the data, as called for by claim 1 of the present invention. Additionally, Appellant's argument is bolstered by the fact that the decoding of the data in ***McKaughan*** or ***Wey*** is certainly not related to the of data size. In fact, the decoding of the data in ***Wey*** refers to matching the frame buffer data with data in the

pattern register. *See* column 2, lines 31-35. Only then does ***Wey*** determine whether the prerequisite number of pattern count has been reached in the pattern counter. Therefore, there is absolutely no reference or suggestion as the size of the data being used as a factor for decoding the data, as called for by claim 1 of the present invention. Hence, ***Wey*** does not disclose or make obvious detecting the size of the data. Further, ***Wey*** simply does not disclose using the size of the data as a factor for decoding the data, as called for by claim 1 of the present invention. Therefore, neither ***McKaughan*** nor ***Wey*** provide disclosure to make obvious the element of detecting the size of the received data's set of signals. Therefore, adding the disclosure of ***Wey*** to ***McKaughan*** does not make obvious all of the elements of claim 1 of the present invention. Accordingly, all of the elements of independent claim 1, 23, 32, and 34 are allowable for at least the reasons cited herein.

Additionally, method claim 32, which also calls for detecting the size of the received data signal for use as a factor for decoding, is allowable since all of its elements are not anticipated or made obvious by ***McKaughan***. Therefore, claim 32 is allowable for at least the reasons cited herein. Additionally, claims 23 and 34, which call for various apparatuses for detecting the size of the received data signal for use as a factor for decoding, are also allowable over ***McKaughan***, ***Wey***, or their combination, for at least the reasons cited herein. Therefore, claims 23 and 34 are also allowable for at least the reasons cited above.

Independent claims 1, 23, 32 and 34 are allowable for at least the reasons cited herein. Additionally, dependent claims 2-9, 24-31, and 35, which respectively depend from independent claims 1, 23, and 34 are also allowable for at least the reasons cited herein.

Further, the Examiner has provided no evidence or arguments as to any reasonable expectation of success that may be found in the prior art, which is a requirement in showing a

prima facie case of obviousness. *In re Vaeck* 947 F.2d 488. Also, the present application disclosed exemplary advantages including the advantage of reducing software operation and full network card operation to maintain the sleep mode and wake-up features for waking up the host circuitry. *See* Specification, page 8, lines 16-23; page 10, lines 4-13. The Examiner provided no evidence as to any such advantages of the cited prior art. This is yet another indication that the novel features called for by claims of the present invention would not have been obvious to those skilled in the art at the time of the invention. Additionally, as described above, the combination of ***McKaughan*** and ***Wey*** do not teach or suggest all the claim limitations, which is another requirement in showing a *prima facie* case of obviousness. *Id.* Accordingly, the Examiner has failed to show a *prima facie* case of obviousness of the claims of the present invention.

B. Claims 3-6, 8, 10-18, 20-22, 25-28, 30, 33 and 35 Are Not Rendered Unpatentable under 35 U.S.C. § 103(a) by *McKaughan* (U.S. Patent No. 5,802,305) in view of *Wey* (U.S. Patent No. 6,098,100) and further in view of *Warren* (US 4,516,201)

The Examiner rejected claims 3-6, 8, 10-18, 20-22, 25-28, 30, 33 and 35 under 35 U.S.C. 103(a) as being unpatentable over ***McKaughan*** in view of ***Wey*** and further in view of ***Warren*** (US 4,516,201). Appellant respectfully traverses the rejections.

Contrary to the Examiner's assertions in the Final Office Action dated April 3, 2006, the combination of ***McKaughan*** and ***Wey*** do not teach, disclose or suggest all of the elements of the independent claims of the present invention. The deficit of ***McKaughan*** and ***Wey*** are not made up for by ***Warren***. Appellant respectfully asserts that even with the use of ***Warren,*** the combination of ***McKaughan, Warren*** and ***Wey*** would still not disclose all of the elements of claims of the present invention.

The deficit of ***McKaughan*** and ***Wey*** is not made up for by ***Warren***. For example, ***Warren*** discloses a host 12 that passes data transmitted by a data link 14, which is examined by a controller 10. *See* col. 6, lines 25-36. However, the system disclosed by ***Warren*** does not check for the size of the data signals; it merely converts the received signal from parallel to a serial format. *See* col. 6, lines 25-36. ***Warren*** merely discloses a link 14 that presents the serial string as parallel words to the host 12. *See* col. 6, lines 37-48. ***Warren*** discloses status information regarding the data link 14 being provided to the host 12 to take action, however ***Warren*** does not disclose any status information regarding the size of the received data signal as called for by the claims of the present invention.

The only reference to memory size in ***Warren*** relates to the limitation of the host system. ***Warren*** discloses that the host system may be joined via the controller where memory size, data handling capacity, or speed limitations would otherwise preclude their joining to a data link 14. *See* col. 7, lines 7-17. However, this does not relate to receiving data signals and detecting the size of the received signals and performing the coding and various other steps for waking up a host circuitry as called for by the claims of the present invention.

Warren does not disclose a wake-up sequence called for by the claims of the present invention. ***Warren*** is generally directed towards the data communication link such as a modem providing a queue for data in a controller. This is vastly different from the disclosure of ***McKaughan***, which is directed towards a wake-up sequence. Therefore, without impermissible hindsight, one of ordinary skill in the art would not combine the disclosure of ***McKaughan*** and ***Warren*** to make obvious any of the claims of the present invention. Therefore, it would be improper hindsight to combine the teachings of ***Warren*** with ***McKaughan*** to make obvious any claim of the present invention. However, even if ***McKaughan***, ***Wey***, and ***Warren*** were

combined, as described above, the deficits of ***McKaughan*** are not made up for by ***Warren*** or ***Key***; including the fact that neither ***McKaughan, Wey, Warren***, nor their combination disclose or make obvious detecting the size of the received set of data signals in the context of decoding the receiving signals, and waking up the host circuitry from a sleep mode, as called for by the claims of the present invention.

For at least the reasons cite above, combining ***Warren***, with the disclosure of ***Wey*** and/or ***McKaughan***, would still not result in disclosing or making obvious all of the elements of any of the claims of the present invention. Therefore, claims 3-6, 8, 10-18, 20-22, 25-28, 30, 33, and 35, are not taught, disclosed, or made obvious by ***McKaughan***, ***Wey***, ***Warren***, or their combinations. Accordingly, claims 3-6, 8, 10-18, 20-22, 25-28, 30, 33, and 35 are allowable for at least the reasons cited above.

Additionally, in the Final Office Action dated April 3, 2006, the Examiner argued that those skilled in the art would allegedly combine the teachings of ***Warren*** to ***McKaughan*** to make obvious various claims of the present invention. The Examiner argued that the judgment of obviousness is necessarily a reconstruction based upon hindsight reasoning but allegedly only takes into account the knowledge that was within the level of others skilled at the time the claim invention was made. However, Appellant asserts that it is impermissible hindsight because the Examiner's reasoning is not based upon knowledge that was available to those skilled in the art without having read the present disclosure. ***Warren*** is directed towards data communication link whereas ***McKaughan*** is directed towards a wake up sequence. There is no disclosure in ***McKaughan*** and ***Warren*** that would prompt those skilled in the art to combine them to make obvious all of the elements of claims of the present invention. The Examiner does not provide sufficient evidence to support or point to any disclosure in either ***Warren*** or ***McKaughan*** that

would direct one skilled in the art to combine them to make obvious all of the elements of claims of the present invention. Therefore, Appellant maintains that those skilled in the art, without using impermissible hindsight reasoning, would not combine ***Warren***, ***McKaughan*** and/or ***Wey*** to make obvious any of the claims of the present invention. Accordingly, claims 1-35 are allowable for at least the reasons cited herein.

Hence, there is insufficient evidence to support any contention that any suggestion or motivation exists to prompt one of ordinary skill in the art to modify the reference or to combine reference teachings, which is a requirement to show a *prima facie* case of obviousness. *In re Vaeck*, 947 F.2d 488. Further, as described above, ***McKaughan***, ***Wey***, and ***Warren***, alone or when combined, do not teach or suggest all the claim limitations, which is a requirement to establish a *prima facie* case of obviousness. *Id.* Additionally, the Examiner has provided no evidence or arguments as to any reasonable expectation of success that may be found in the prior art, which is a requirement in showing a *prima facie* case of obviousness. *Id.* Accordingly, the Examiner has failed to show any one of the three prongs to establish a *prima facie* case of obviousness. Accordingly, the Examiner erred in rejection the claims of the present invention.

Appellant acknowledges and appreciates that the Examiner has indicated that claims 7, 19 and 29 contain allowable subject matter. In light of the arguments provided herein, Appellant respectfully asserts that all claims of the present invention are also allowable.

VIII. CLAIMS APPENDIX

The claims currently under consideration, *i.e.*, claims 1-35, are listed in the Claims Appendix submitted herewith.

IX. EVIDENCE APPENDIX

There is no evidence relied upon in this Appeal with respect to this section.

X. RELATED PROCEEDINGS APPENDIX

There are no related appeals and/or interferences that might affect the outcome of this proceeding.

In view of the foregoing, it is respectfully submitted that the Examiner erred in not allowing all claims (claims 1-35) pending in the present application over the prior art of record. **The undersigned attorney may be contacted at (713) 934-4069** with respect to any questions, comments, or suggestions relating to this appeal.

Respectfully submitted,

WILLIAMS, MORGAN & AMERSON, P.C.
CUSTOMER NO. 23720

Date: August 30, 2006

By: _____

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CLAIMS APPENDIX

1. (Previously Amended) A method for detecting and decoding data comprising:

receiving a set of data signals from an external data source;

detecting a size of said received set of data signals to use as a factor for decoding said data;

decoding said received set of data signals;

extracting a destination address from said set of data signals;

comparing said destination address extracted from said data signals to a known data value;

determining whether said received data signals should be received by a host circuitry based upon said comparison of said destination address extracted from said data signals to said known data value;

generating at least one status signal alerting said host circuitry of said determination that said received data signals should be received by said host circuitry; and

waking up said host circuitry from a sleep mode upon a determination that said received set of data is addressed to said host circuitry.

2. (Original) The method as described in claim 1, wherein said set of data signal received is a data packet that is in a serial data format, over a network line.

3. (Previously Amended) The method as described in claim 2, further comprising detecting said size of said received set of data signal and decoding said received set of data signals, detecting and decoding said size of said received set of data signal comprising:

converting a serial data packet into a parallel data format;

extracting a word clock from a received data packet;

incrementing a number held by a counter, said word clock generating a word count;

inputting said converted parallel format data into a plurality of comparators;

using said word count to address data stored in a memory circuitry; and

inputting a set of data signals from said memory circuitry into an appropriate comparator.

4. (Previously Amended) The method as described in claim 3, wherein said act of extracting said destination address from said set of data signals further comprises slicing said parallel data such that at least one destination address data word is generated.

5. (Previously Amended) The method as described in claim 3, wherein said method of comparing said destination address to a known data value further comprises:

performing a comparison function upon said converted parallel set of data signals and said set of data from said memory circuitry;

generating a digital comparator status signal in response of said performance of comparator function; and

clocking in said digital comparator data signal into a register.

6. (Previously Amended) The method as described in claim 5, wherein said method of determining whether said received data signals should be received by said host circuitry further comprises latching all output of said plurality of comparators into a digital logic circuitry.

7. (Original) The method as described in claim 6, wherein said output of said comparators are not latched when a mask circuitry indicates that a particular frame of data is not compared.

8. (Original) The method as described in claim 5, wherein said method of generating a status signal alerting said host circuitry further comprises performing an OR function upon all said latched output of said comparators.

9. (Previously Amended) The method as described in claim 1, wherein said method of waking up said host circuitry further comprises generating a status signal alerting said host circuitry that a address match has been found.

10. (Previously Amended) An apparatus for detecting and decoding data, comprising:

means for receiving a data signal;

means for detecting a size of said received data signal;

a data formatter;

a clock divider;

a counter;

a host circuitry interface capable of transmitting and receiving data from a host circuitry, said host circuitry enter a wake up state from a sleep mode based upon decoded address data received by said host circuitry, said decoded address data being based_upon a content of_said data signal and said size of said received data signals;

a memory circuitry;

a plurality of comparators;

a mask circuitry;

a digital logic circuitry;

a plurality of status registers; and

a plurality of clocked registers.

11. (Original) The apparatus as described in claim 10, wherein said data formatter comprises of a serial to parallel converter and a data end detector that are capable of converting a serial stream of data into parallel data words and detecting an end of a data stream.

12. (Original) The apparatus as described in claim 10, wherein said clock divider is capable of incrementing a count held by said counter.

13. (Original) The apparatus as described in claim 10, wherein said memory circuitry comprises of a memory element and a memory data access logic.

14. (Original) The apparatus as described in claim 13, wherein said memory element is coupled with said memory data access logic such that data from said memory element can be retrieved and sent through said memory data access logic.

15. (Original) The apparatus as described in claim 14, wherein said memory data access logic is coupled with said host interface such that data can be sent to and retrieved from said memory elements.

16. (Original) The apparatus as described in claim 10, wherein said comparators are coupled with said data formatter such that said comparators receive parallel formatted data from said data formatter.

17. (Original) The apparatus as described in claim 16, wherein said comparators are further coupled with said memory circuitry such that said comparator is capable of receiving data from said memory circuitry.

18. (Original) The apparatus as described in claim 17, wherein at least one output from said comparators is further coupled to said digital logic circuitry and said clock registers

such that said output of said comparators is latched by said digital logic circuitry and said clock registers.

19. (Original) The apparatus as described in claim 18, wherein said mask circuitry is capable of preventing a registering of said comparator output into said clocked registers.

20. (Original) The apparatus as described in claim 18, wherein said status registers are coupled to said digital logic circuitry and said clocked registers such that said latched comparator outputs are inputted into said status registers.

21. (Original) The apparatus as described in claim 10, wherein an output from said digital logic circuitry is clock-registered by a signal output from said data formatter.

22. (Previously Amended) The apparatus as described in claim 10, wherein said status registers are coupled with said host interface such that data from said status register could be retrieved through an access port.

23. (Previously Amended) A computer readable program storage device encoded with instructions that, when executed by a computer, performs a method, comprising:

receiving a set of data signals from an external data source;

detecting a size of said received set of data signals to use as a factor for decoding said data signals;

decoding said received set of data signals;

extracting a destination address from said set of data signals;

comparing said destination address extracted from said data signals to a known data value;

determining whether said received data signals should be received by a host circuitry based upon said comparison of said destination address extracted from said data signals to said known data value;

generating at least one status signal alerting said host circuitry of said determination that said received data signals should be received by said host circuitry; and

waking up said host circuitry from a sleep mode upon a determination that said received set of data is addressed to said host circuitry.

24. (Previously presented) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 23, wherein said set of data signal received is a data packet that is in a serial data format, over a network line.

25. (Previously Amended) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 24, further comprising detecting said size of said received set of data signal and decoding said received set of data signals, detecting and decoding said size of said received set of data signal comprising:

converting said serial data packet into a parallel data format;

extracting a word clock from said received data packet;

incrementing a number held by said counter, said word clock generating a word count;

inputting said converted parallel format data into a plurality of comparators;

using said word count to address data stored in a memory circuitry; and

inputting a set of data signals from said memory circuitry into an appropriate comparator.

26. (Previously Amended) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 25, wherein said act of extracting said destination address from said set of data signals further comprises slicing said parallel data such that at least one destination address data word is generated.

27. (Previously Amended) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 25, wherein said method of comparing said destination address to said known data value further comprises:

performing a comparison function upon said converted, parallel set of data signals, and said set of data from said memory circuitry;

generating a digital comparator status signal in response of said performance of comparator function; and

clocking in said digital comparator data signal into a register.

28. (Previously Amended) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 27, wherein said method of determining whether said received data signals should be received by said host circuitry further comprises latching all output of said plurality of comparators into a digital logic circuitry.

29. (Previously presented) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 28, wherein said output of said comparators are not latched when a mask circuitry indicates that a particular frame of data is not compared.

30. (Previously presented) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 28, wherein said method of generating a status signal alerting said host circuitry further comprises performing an OR function upon all said latched output of said comparators.

31. (Previously Amended) The computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 23, wherein said method of waking up said host circuitry further comprises generating a status signal alerting said host circuitry that a address match has been found.

32. (Previously Amended) A method, comprising:

receiving a data signal;

detecting a size of said received data signal to use as a factor for extracting a destination address;

extracting said destination address based upon said data signal to determine whether a host circuitry is being addressed by comparing said destination address to a predetermined address; and

waking up said host circuitry from a sleep mode based upon said determination that said host circuitry is being addressed.

33. (Previously Amended) The method of claim 32, wherein extracting said destination address further comprises:

converting a serial data packet from said received data into a parallel data format;

extracting a word clock from said received data packet;

incrementing a number held by a counter, said word clock generating a word count;

inputting said converted parallel format data into a plurality of comparators;

using said word count to address data stored in a memory circuitry;

inputting a set of data signals from said memory circuitry into an appropriate comparator; and

extracting said destination address by slicing said parallel data such that at least one destination address data word is generated.

34. (Previously Amended) An apparatus, comprising a controller to:

receive a data signal;

detect a size of said received set of data signals to use as a factor to extract a destination address;

extract said destination address based upon said data signal to determine whether a host circuitry is being addressed by comparing said destination address to a predetermined address; and

wake up said host circuitry from a sleep mode based upon said determination that said host circuitry is being addressed.

35. (Previously Amended) The apparatus of claim 34, further comprising:

a data formatter capable of converting a serial stream of data into parallel data words and detecting an end of a data stream;

a counter to receive parallel formatted data from said data formatter;

a clock divider capable of incrementing a count held by a counter;

a memory circuitry comprising a memory element and a memory data access logic;

a plurality of comparators to receive parallel formatted data from said data formatter;

a plurality of clocked registers;

a mask circuitry capable of preventing a registering of said comparator output into said clocked registers; and

a plurality of status registers to latch an output from said comparators.